

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A switch circuit comprising:

at least two input terminals and one output terminal,
first switches, each first switch comprising a first and second port, each first switch being electronically switchable between a first state, wherein the first port is disconnected from the second port, and a second state, wherein the first port is connected to the second port, wherein each of the input terminals is connected to a first port of a respective one of said first switches, and

a second switch with at least two branch ports and a common port coupled to said output terminal, said second switch electronically switchable between different states, wherein in each state ~~one~~ a respective branch port of the at least two branch ports is connected to the common port and the ~~rest~~ remainder of the at least two branch ports are disconnected from the common port, wherein each of the branch ports is connected to a second port of a corresponding one of said first switches;

wherein the first switches are configured so that all of the first switches are not in the first state simultaneously, wherein one of the at least two input terminals is connected to a terrestrial TV antenna and another of the at least two input terminals is connected to a TV cable network, wherein one of the first switches receives a first TV signal from the terrestrial TV antenna and another of the first switches receives a second TV signal from the TV cable network.

2. (canceled)

3. (canceled)

4. (previously presented) Circuit according to claim 1, wherein the first switches are comprised of discrete electronic parts.

5. (previously presented) Circuit according to claim 1, wherein the second switch is an integrated circuit.

6. (previously presented) Circuit according to claim 1, wherein a control circuit is provided to synchronously control said first switches and said second switch.

7. (canceled)

8. (previously presented) Circuit according to claim 6, wherein the control circuit is connected to an I²C transceiver.

9. (canceled)

10. (currently amended) A receiver circuit for receiving a radio frequency signal, the receiver circuit comprising:

at least two radio frequency input terminals;

a tuner circuit for receiving radio frequency signals at an input, and for generating baseband signals; and

a switch circuit comprising:

at least two input terminals and one output terminal,

first switches, each first switch comprising a first and second port, each first switch being electronically switchable between a first state, wherein the first port is disconnected from the second port , and a second state, wherein the first port is connected to the second port , wherein each of the input terminals is connected to a first port of a respective one of said first switches, and

a second switch with at least two branch ports and a common port coupled to said output terminal, said second switch electronically switchable between different states, wherein in each state ~~one~~ a respective branch port of the at least two branch ports

is connected to the common port and the ~~rest~~ remainder of the at least two branch ports are disconnected from the common port, wherein each of the branch ports is connected to a second port of a corresponding one of said first switches,

wherein the input terminals are connected to the radio frequency input terminals and the output terminal is connected to the input of the tuner, wherein the first switches are configured so that all of the first switches are not in the first state simultaneously, wherein one of the at least two radio frequency input terminals is connected to a terrestrial TV antenna and another of the at least two radio frequency input terminals is connected to a TV cable network, wherein one of the first switches receives a first TV signal from the terrestrial TV antenna and another of the first switches receives a second TV signal from the TV cable network.

11. (previously presented) The receiver circuit of claim 10, wherein the first switches are implemented using PIN diodes.

12. (previously presented) The receiver circuit of claim 11, wherein the first switches are implemented using two anti-parallel PIN-diodes in series connection between the respective first and second ports, and wherein a driver terminal is connected between the diodes.

13. (canceled)

14. (canceled)

15. (previously presented) The receiver circuit of claim 10, wherein a control circuit is provided to synchronously control said first switches and said second switch.

16. (canceled)

17. (canceled)

18. (canceled)

19. (canceled)

20. (canceled)

21. (canceled)

22. (canceled)

23. (canceled)

24. (previously presented) Circuit according to claim 1, wherein the first switches are implemented using PIN diodes.

25. (previously presented) Circuit according to claim 1, wherein the first switches are implemented using two anti-parallel PIN-diodes in series connection between the respective first and second ports, and wherein a driver terminal is connected between the diodes.

26. (canceled)

27. (previously presented) Circuit according to claim 6, wherein the control circuit comprises a control terminal, a first driver circuit, and a second driver circuit, wherein the first driver circuit provides a first voltage signal to drive one of the first switches, wherein the second driver circuit provides a second voltage signal to drive another of the first switches, wherein the first voltage signal is an inversion of the second voltage signal, the first voltage signal and the second voltage signal being generated from a voltage signal provided at the control terminal.

28. (previously presented) Circuit according to claim 27, wherein the control circuit further comprises a resistive divider network coupled to the first driver circuit, the resistive divider network being configured to obtain a third voltage signal from the first voltage signal and to control the second switch using the third voltage signal.
29. (previously presented) The receiver circuit of claim 15, wherein the control circuit comprises a control terminal, a first driver circuit, and a second driver circuit, wherein the first driver circuit provides a first voltage signal to drive one of the first switches, wherein the second driver circuit provides a second voltage signal to drive another of the first switches, wherein the first voltage signal is an inversion of the second voltage signal, the first voltage signal and the second voltage signal being generated from a voltage signal provided at the control terminal.
30. (previously presented) The receiver circuit of claim 29, wherein the control circuit further comprises a resistive divider network coupled to the first driver circuit, the resistive divider network being configured to obtain a third voltage signal from the first voltage signal and to control the second switch using the third voltage signal.
31. (previously presented) The receiver circuit of claim 10, wherein the tuner circuit includes an I²C transceiver configured to receive commands via an I²C bus and to use the commands to control the switch circuit.
32. (canceled)
33. (currently amended) A receiver set comprising a set top box and a TV device coupled to the set top box, wherein the set top box includes the receiver circuit of claim 32_10.
34. (currently amended) A computer system comprising a TV card and a computer monitor coupled to the TV card, wherein the TV card includes the receiver circuit of claim 32_10.

35. (new) A switch circuit comprising:

at least two input terminals and one output terminal,
first switches, each first switch comprising a first and second port, each first switch being electronically switchable between a first state, wherein the first port is disconnected from the second port, and a second state, wherein the first port is connected to the second port, wherein each of the input terminals is connected to a first port of a respective one of said first switches, and

a second switch with at least two branch ports and a common port coupled to said output terminal, said second switch electronically switchable between different states, wherein in each state a respective branch port of the at least two branch ports is connected to the common port and the remainder of the at least two branch ports are disconnected from the common port, wherein each of the branch ports is connected to a second port of a corresponding one of said first switches;

wherein the first switches are configured so that all of the first switches are not in the first state simultaneously, wherein a control circuit is provided to synchronously control said first switches and said second switch, wherein the control circuit comprises a control terminal, a first driver circuit, and a second driver circuit, wherein the first driver circuit provides a first voltage signal to drive one of the first switches, wherein the second driver circuit provides a second voltage signal to drive another of the first switches, wherein the first voltage signal is an inversion of the second voltage signal, the first voltage signal and the second voltage signal being generated from a voltage signal provided at the control terminal, wherein the control circuit further comprises a resistive divider network coupled to the first driver circuit, the resistive divider network being configured to obtain a third voltage signal from the first voltage signal and to control the second switch using the third voltage signal.

36. (new) Circuit according to claim 35, wherein the first switches are implemented using PIN diodes.